IN THE DRAWINGS:

Applicants are submitting herewith corrected Figures 3 – 6. Applicants have attached both "Annotated Marked Up Drawings" and "Replacement Sheets" for the Examiner's convenience.

REMARKS

In the Office Action, the Examiner allowed all of the pending claims, which are claims 8 and 10-12, however the Examiner raised objections to the specification and the drawings.

With respect to the drawings, the Examiner noted that the reference numbers "30" and "44" are shown in the figures, but not mentioned in the description, and that the two rightmost vertical arrows in Fig. 3 should be labeled "100." The Examiner also observed that Figs. 4 and 5 both include a top center arrow that is not labeled or described in the specification, and that in Fig. 6, the "40" should be "42."

With respect to the specification, the Examiner noted that in paragraph 20, "gate region" should be "gate stack," and the Examiner commented that the language of paragraph 23 is inconsistent and confusing.

Applicants' Attorneys have carefully reviewed the entire application, including the specification and the drawings, and several editorial changes are being made to the specification and the drawings. It is believed that these changes fully address the objections raised by the Examiner.

More specifically, in the drawings, in Figure 3, the rightmost arrows are being labeled "100," and in Figures 4 and 5, the top center arrows are being deleted. Further, in Figure 5, the reference number "44" has been removed, and in Figure 6, the reference number "42" has been changed to "44." Also, the specification, in paragraph 24 is being amended to reference the extension regions 30 shown in Figures 3, 4 and 5.

Paragraphs 20, 23, 24 and 25 are being amended to improve their readability. For instance, in paragraph 20, "gate region" is being changed, as the Examiner requested, to "gate stack." Paragraph 23 is being amended to refer more consistently to "gate stack" "liner 24," and "spacer 26."

With particular regard to paragraph 23, Applicants note that the reference to the layer 22 being added and the reference to the spacer 24 being formed, is in the context of the explanation of why these elements were formed – to keep the doping implantation away from the certain regions of the semiconductor device. In order to improve the readability of the paragraph, the language that the disposable layer "is added" is being changed to "was added," and the language that the spacer 26 "is formed" is being changed to "was formed."

With the above-discussed changes to the drawings and to the specification, all of the reference numbers in the drawings are referred to in the specification, and all of the reference numbers mentioned in the specification are shown in the drawings. Further, the description of the way in which the method of this invention is practiced is easier to read and to understand.

For the reasons set forth above, the Examiner is requested to reconsider and to withdraw the objections to the drawings and to the specification.

Every effort has been made to place this application in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,

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FIG. 3

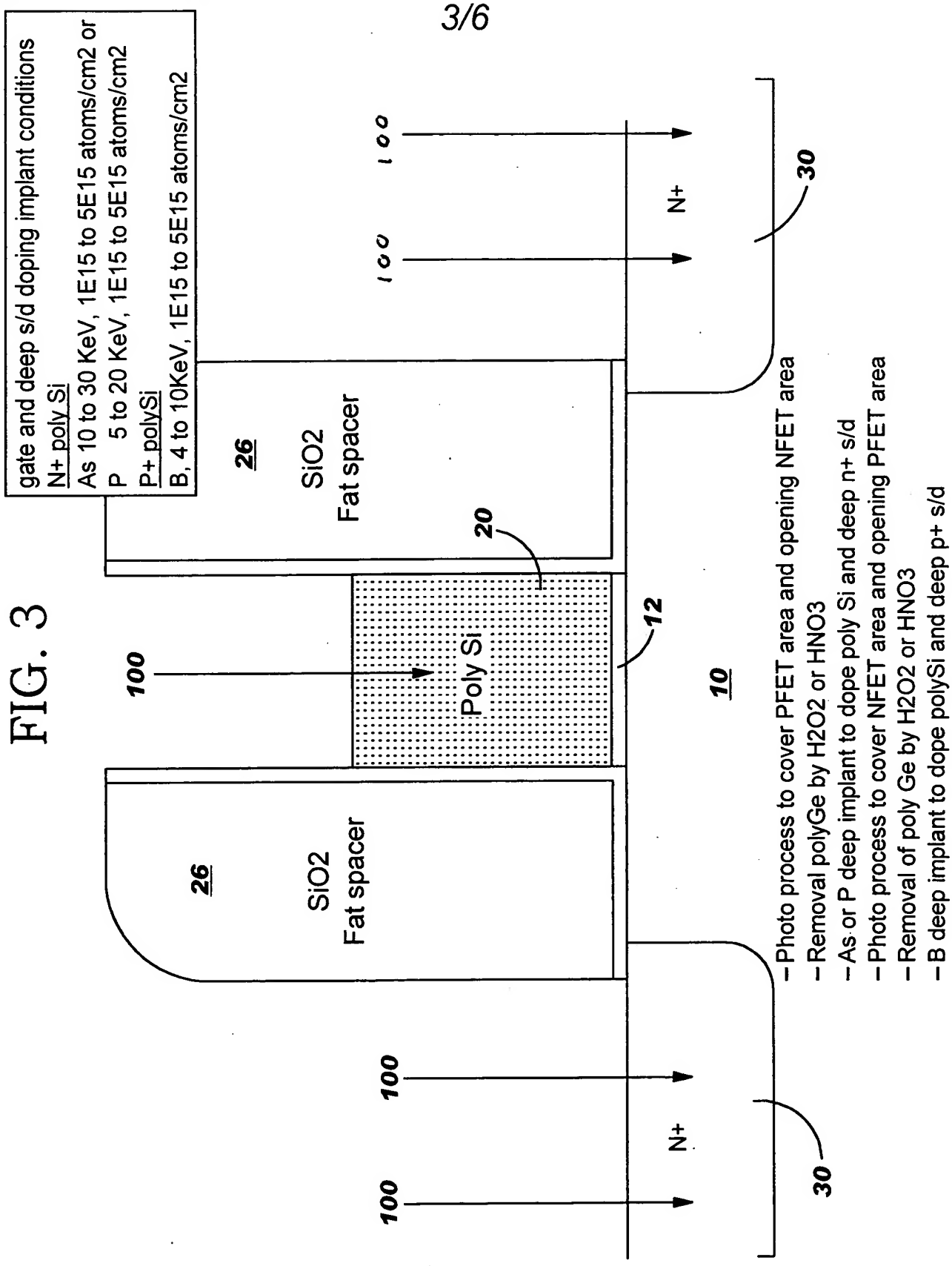


FIG. 4

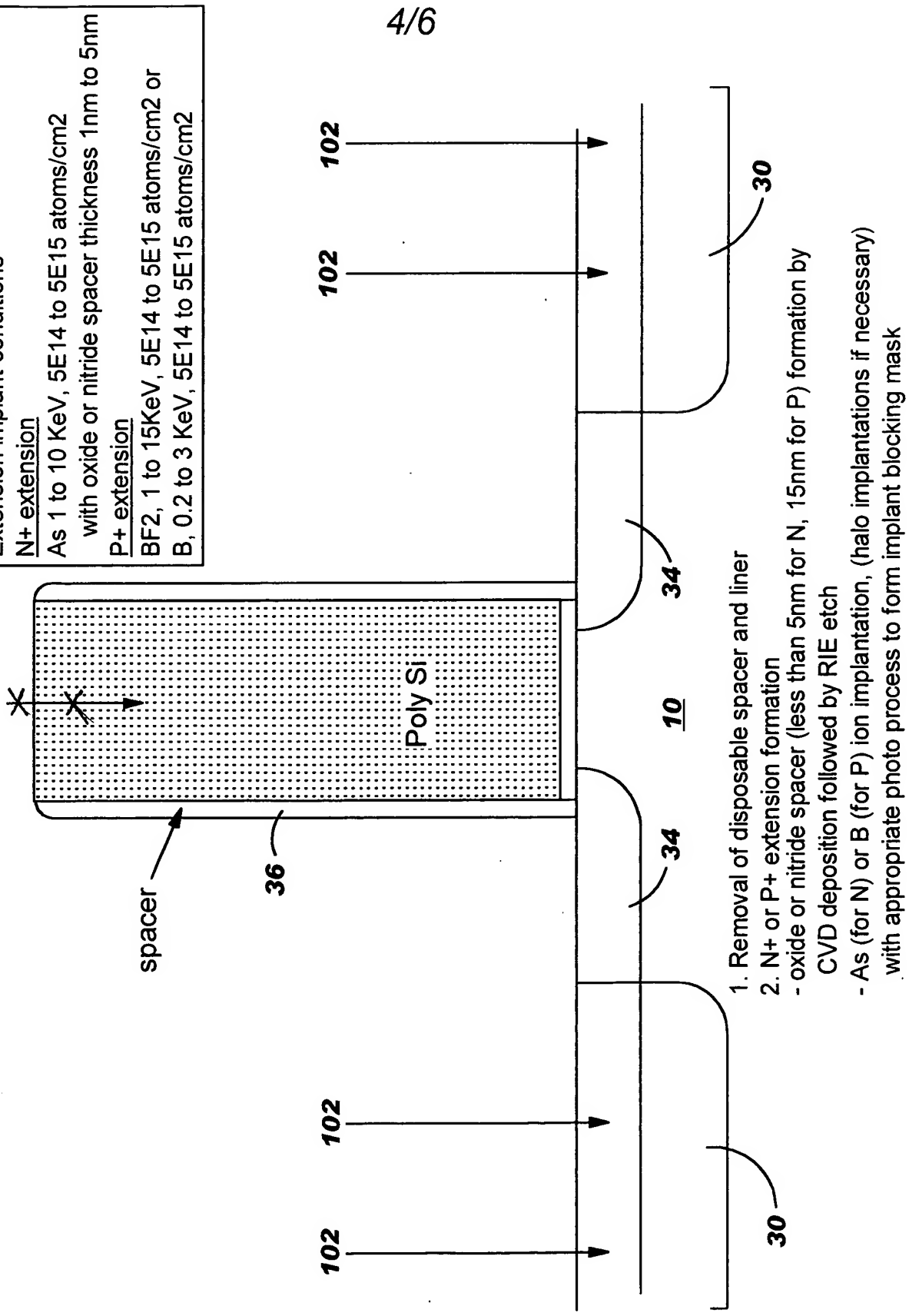
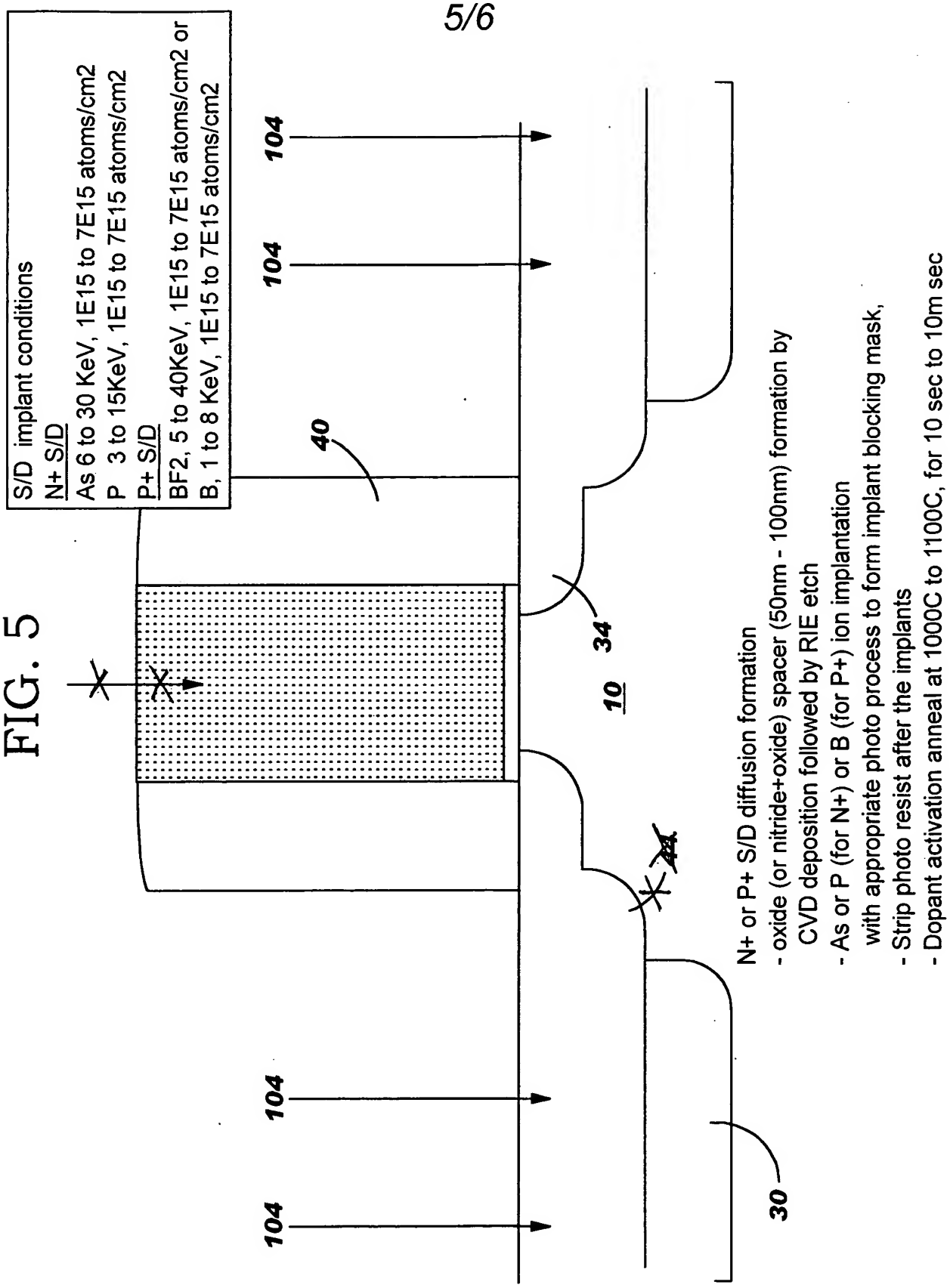

Extension implant conditions
N+ extension
As 1 to 10 KeV, 5E14 to 5E15 atoms/cm2
with oxide or nitride spacer thickness 1nm to 5nm
P+ extension
BF2, 1 to 15KeV, 5E14 to 5E15 atoms/cm2 or
B, 0.2 to 3 KeV, 5E14 to 5E15 atoms/cm2
102
102
102
102
30
30
34
34
10
Poly Si
36
spacer
1. Removal of disposable spacer and liner
2. N+ or P+ extension formation
- oxide or nitride spacer (less than 5nm for N, 15nm for P) formation by CVD deposition followed by RIE etch
- As (for N) or B (for P) ion implantation, (halo implantations if necessary) with appropriate photo process to form implant blocking mask

FIG. 5


S/D implant conditions
N+ S/D
As 6 to 30 KeV, 1E15 to 7E15 atoms/cm2
P 3 to 15KeV, 1E15 to 7E15 atoms/cm2
P+ S/D
BF2, 5 to 40KeV, 1E15 to 7E15 atoms/cm2 or
B, 1 to 8 KeV, 1E15 to 7E15 atoms/cm2
104
104
104
104
40
34
10
44
30
N+ or P+ S/D diffusion formation
- oxide (or nitride+oxide) spacer (50nm - 100nm) formation by CVD deposition followed by RIE etch
- As or P (for N+) or B (for P+) ion implantation with appropriate photo process to form implant blocking mask,
- Strip photo resist after the implants
- Dopant activation anneal at 1000C to 1100C, for 10 sec to 10m sec

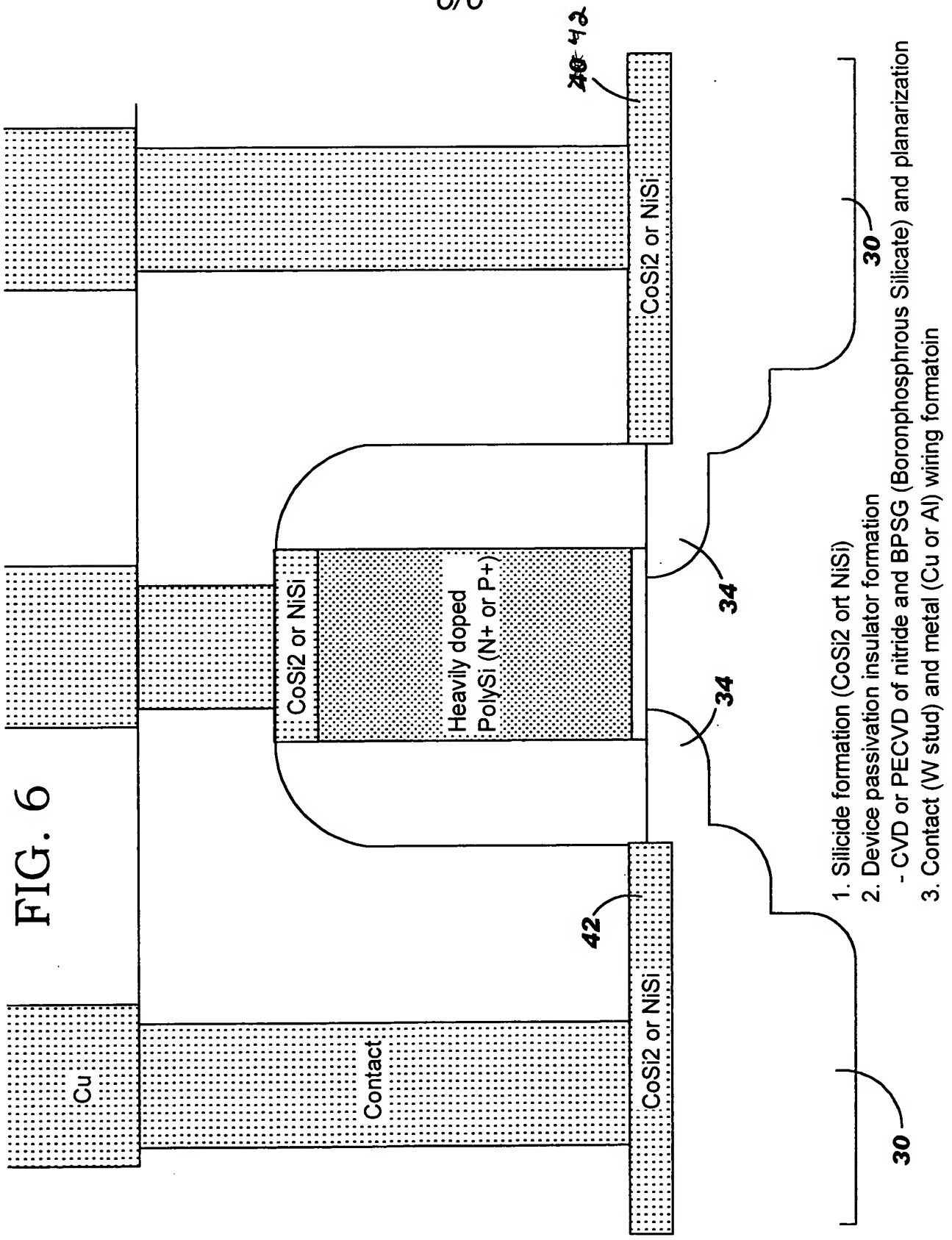

CoSi2 or NiSi
CoSi2 or NiSi
Heavily doped
PolySi (N+ or P+)
CoSi2 or NiSi
Contact
Cu
42
42
34
34
30
30
1. Silicide formation (CoSi2 ort NiSi)
2. Device passivation insulator formation
- CVD or PECVD of nitride and BPSG (Boronphosphrous Silicate) and planarization
3. Contact (W stud) and metal (Cu or Al) wiring formatoin

FIG. 6